Claims

1. Claims 1-24 remain for examination. Claims 25-28 are newly added.

2. This is action included new point of arguments which were not clearly set forth in the last office action by previous examiner. Therefore, it is a non-final action in order to allow applicant a chance to respond. Response to applicant's remarks will be included herein.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless-

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21 (2) of such treaty in the English language.

Claims 1-9, 13-17, and 21-24, 25-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Keller (6,622,237).

As to the amended feature of new load instruction is admitted in claim 1, examiner holds that any input load instruction is a new load admitted instruction (see Keller's load instructions received by decoder 24 in col.10, lines 40).

As to claim 14, Keller also included at least a new load instruction (see the younger loads in col.11, lines 45-49).

As to claims 22,24, the change of uops tom microinstructions does not change the original scope of claim.

As to new claim 25, see the dependency between the load and store instructions in col.10, lines 34-46).

As to new claim 26, Keller also calculated store address (see how the operands added produce virtual address of a store operation in col.11, lines 61-67, col.12, lines 1-6).

As to new claim 27, Keller also taught at least :

a) decoding a store instruction as a plurality of microinstructions, including an STA and a corresponding STD microinstruction (see decoding of store and load instructions in col.5, lines 28-56, col.6, lines 25-40),

b) decoding a load instruction as at least one load microinstruction, when a dependency between the STA microinstruction and the load microinstruction occurs (see the dependency between the load and store instructions in col.10, lines 34-46), deferring scheduling of the load microinstruction until after the corresponding STD

microinstruction executes (see load instruction does not get scheduled prior to the store in col.10, lines 40-46, see also the retry of the load on matching condition with the store in col.12, lines 11-22).

As to claim 28, Keller also detected the dependency between the STA microinstruction (see store instruction) and the load microinstruction (see load instruction) by comparing an identifier (see match found of physical address col.12, lines 10-22)of the STD microinstruction to dependency pointers of other microinstructions stored by a scheduler (66,70), and clearing any dependency pointers that match the identifier (see the operation state being reset) .

Claims 10-12 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller in view of Abramson (5,898,854) and Hennessy (Computer Organization and Design).

As to amended claims 10,18, Keller also included first plurality (see load instructions) and second plurality (store instructions, see older stores in col.11, lines 52).

As to claim 19, see dependencies form dependency unit 62 in col.10, lines 30-55).

The rejections are maintained and incorporated by reference the last Office action 06/16/04.

The response filed on 09/16/04 has been fully considered but is not persuasive.

In the remarks, applicant argued that :

a) Keller did not teach when a new load instruction is admitted, predicting whether collision occurs between the load microinstruction and an older store microinstruction,

b) predicting whether a new load microinstruction collides with a first previously received store microinstruction when the new load microinstruction is admitted to a scheduler.

As to a) above, Keller teaches when a new load instruction is admitted, predicting whether collision (see the dependency determination of load and store) occurs between the load microinstruction and an older store microinstruction (see col.10, lines 35-46).

As to b), Keller also taught predicting whether a new load microinstruction collides with a first previously received store microinstruction (see the dependency of the load instruction with previous store instruction by the predictor 60 and scheduler 66 in col.10, lines 1-46) when the new load microinstruction is admitted to a scheduler (see scheduler 66).

Keller(6,622,237) , Abramson (5,898,854) and Hennessy (Computer Organization and Design) were already cited in 892 in previous office action on 06/16/04.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

/Daniel Pan/
Primary Examiner, Art Unit 2183